Remarks

The applicants have carefully considered the final Office action dated May 31, 2007. In view of the forgoing amendments and the following remarks, reconsideration of the application is respectfully requested.

As an initial matter, claims 1-4 and 10-19 have been cancelled to place the application in better form for appeal. The applicants respectfully request that the amendments be admitted to the record to simplify the issues to be appealed.

Turning to the rejections of the remaining claims, in the final Office action, claims 5-7 and 20-22 were rejected as unpatentable over Ju (US 6,260,190) in view of McKinsey (US 6,463,579) and Babaian (US 7,065,750). Claims 8, 9, 23, and 24 were rejected as unpatentable over Ju in view of McKinsey.

Claim 5 recites a method comprising, *inter alia,* determining a second instruction in the plurality of instructions that computes a previous value of a target register associated with the first instruction when the first instruction is not an excepting instruction and the first instruction is to be moved upward across a check instruction.

In the Response to Arguments section of the final Office action dated May 31, 2007, the examiner recognizes that the applicants specification defines an "excepting instruction" as "an instruction that may cause an exception to occur." (Specification, ¶ [0025]). The examiner further admits in the Office action that such a definition is "a reasonable interpretation." Therefore, an instruction that is capable of generating an exception is clearly an excepting instruction.

In rejecting claim 5, the examiner argues in the final Office action that Ju describes "moving a first instruction that is not an excepting instruction upward across a check instruction (see, for example, column 28, lines 10-51, which shows moving the first add

instruction upward across a check instruction, and which shows that the load instruction is the excepting instruction." (final Office action, Page 9, ¶ 1). In the Response to Arguments section of the final Office action, the examiner argues "Ju does not indicate that the add instruction ever generates an exception." (final Office action Page 3, lines 18-19). However, the examiner's contention is incorrect. Ju clearly describes that an add instruction is capable of generating an instruction in the following paragraph:

> The instruction "ADD," declared on line 47, is an add instruction that adds the contents of the registers "i" and "j" and places the result in the register "dest." The instruction "ADD.E," declared on line 48, is an eager-mode variation of the previously declared add instruction. Most instructions in the PlayDoh architecture have eager-mode equivalents. If none of the speculative tags associated with the source registers of an eager-mode instruction, registers "i" and "j" in the case of the ADD.E instruction, are set, then execution of the instruction proceeds normally when the instruction does not generate an exception. When the instruction does generate an exception, the instruction sets the speculative tag of the destination register to TRUE, but does not signal the exception. If, on the other hand, the speculative tag of one or more of the source registers are set, then the instruction does not execute, but instead sets the speculative tag of the destination register. Thus, an eager-mode instruction defers the signaling of an exception generated during execution of the instruction and propagates an exception that was generated by a previously executed instruction by copying the speculative tag from source registers to the destination register. ***Non-eager-mode instructions immediately signal exceptions that are generated during execution of the instruction and immediately signal the exception associated with a source register having a speculative tag set to TRUE. Thus, non-eager-mode instructions neither defer nor propagate exceptions.***

(Ju, Col. 17, line 52-Col. 18, line 11) (emphasis added). The italicized portions of the above quotation clearly indicates that an add instruction is an excepting instruction. Accordingly, a fundamental premise of the rejection is plainly in error and the rejection will be reversed on appeal.

Further, the deficiencies of Ju are not addressed by the cited portions of McKinsey or Babaian. Therefore, the rejection is clearly in error and the applicants respectfully request that the rejection of claim 5 and all claims depending therefrom be withdrawn.

The applicants also note that the examiner has incorrectly characterized the remarks of the applicants by suggesting that the applicants acknowledge that Ju does not indicate that an add instruction ever generates an exception. (Page 3, lines 18-19). For supporting this suggestion, the examiner points to the following remark in the applicants response to the Office action dated October 4, 2006: "However, while the add instruction may not be described as generating an exception during the particular execution example described in Ju, ***an add instruction is inherently an excepting instruction***." (Applicants response dated March 5, 2007, page 11, lines 19-21) (emphasis added here). As shown by the quotation, the applicants were referring to Ju's description of a particular example in which the add instruction did not cause an exception to occur. The fact that an add instruction did not cause an exception in a particular example does not foreclose the possibility of the add instruction ever throwing an exception. In fact, as described and cited above, Ju unmistakably indicates that an add instruction is an excepting instruction.

In the Office action, claim 8 was rejected as unpatentable over Ju in view of McKinsey. Claim 8 recites a method comprising inserting a copy of the first instruction into a recovery block if (i) the first instruction is not an excepting instruction, (ii) the first instruction is not to be moved upward across a check instruction, and (iii) the first instruction is to be moved downward across a check instruction. As described above in connection with claim 5, Ju, McKinsey, and Babaian whether taken alone or in combination fail to describe or suggest that the first instruction is not an excepting instruction. Therefore, claim 8 and all claims depending therefrom are in condition for allowance.

In the Office action, claim 20 was rejected as unpatentable over Ju in view of McKinsey and Babaian. Claim 20 recites a machine readable medium structured to cause a machine to, *inter alia*, determine a second instruction in the plurality of instructions that computes a previous value of a target register associated with the first instruction when the first instruction is not an excepting instruction and the first instruction is to be moved upward across a check instruction. As described above in connection with claim 5, Ju, McKinsey, and Babaian whether taken alone or in combination fail to describe or suggest that the first instruction is not an excepting instruction. Therefore, claim 8 and all claims depending therefrom are in condition for allowance.

In the Office action, claim 23 was rejected as unpatentable over Ju in view of McKinsey. Claim 23 recites a machine readable medium structured to cause a machine to determine if the first instruction is an excepting instruction and insert a copy of the first instruction into a recovery block in response to determining that (i) the first instruction is not an excepting instruction, (ii) the first instruction is not to be moved upward across a check instruction, and (iii) the first instruction is to be moved downward across a check instruction. As described above in connection with claim 5, Ju, McKinsey, and Babaian whether taken alone or in combination fail to describe or suggest that the first instruction is not an excepting instruction. Therefore, claim 23 and all claims depending therefrom are in condition for allowance.

Reconsideration of the application and allowance thereof are respectfully requested. If there is any matter that the examiner would like to discuss, the examiner is invited to contact the undersigned representative at the telephone number set forth below.

Respectfully submitted,

HANLEY, FLIGHT & ZIMMERMAN, LLC
150 S. Wacker Dr.
Suite 2100
Chicago, Illinois 60606

Dated: **July 31, 2007**

/Michael W. Zimmerman/

Michael W. Zimmerman
Reg. No. 57,993
Agent for Applicants
312.580.1020